

IN THE DRAWINGS

Applicant is submitting replacement drawing sheets to amend Figures 7B, 9, 10, 11, 12, 13A, 13B, 13C, and 14. The amendment to the drawings removes equations from the Figure 7B, removes the tables in Figures 9-11, renumbers Figures 12, 13A, 13B, 13C and 14 as Figures 9, 10A, 10B, 10C and 11, respectively, and renumbers the reference numbers in Figure 14 to correspond to renumbered Figure 11. The specification includes the substance of the text removed from the drawings. Applicant respectfully asserts that no new matter has been added to the application. Since the number of drawings has changed, Applicant is submitting replacement drawing sheets for all of the Figures.



1/17

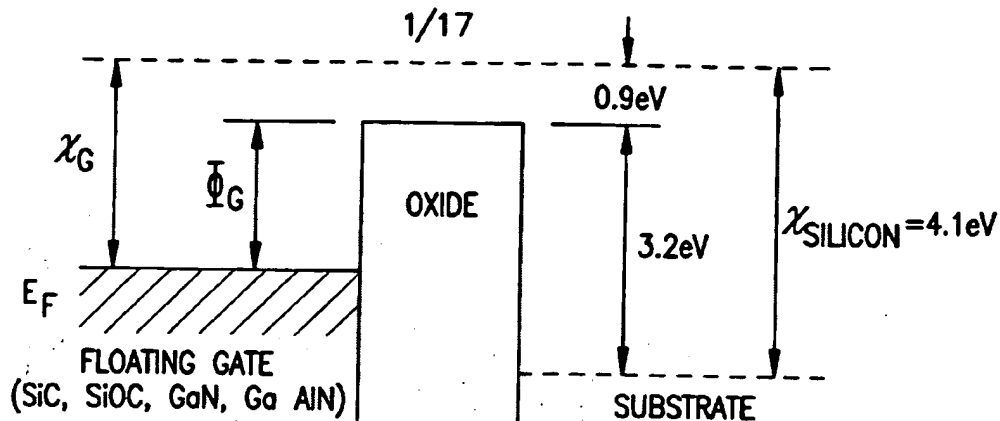


FIG. 1A
 (PRIOR ART)

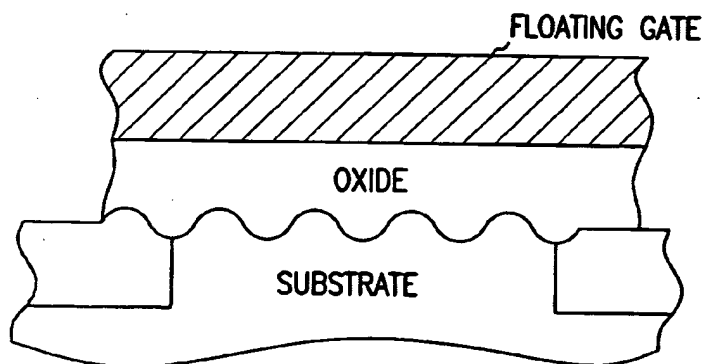


FIG. 1B
 (PRIOR ART)

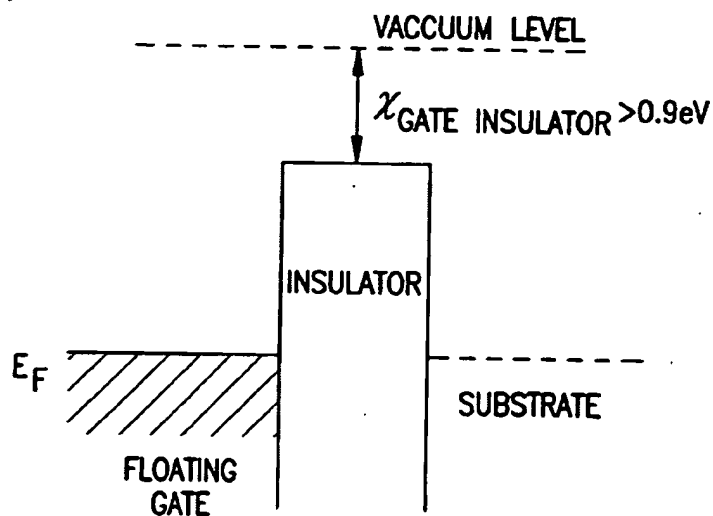


FIG. 1C
 (PRIOR ART)

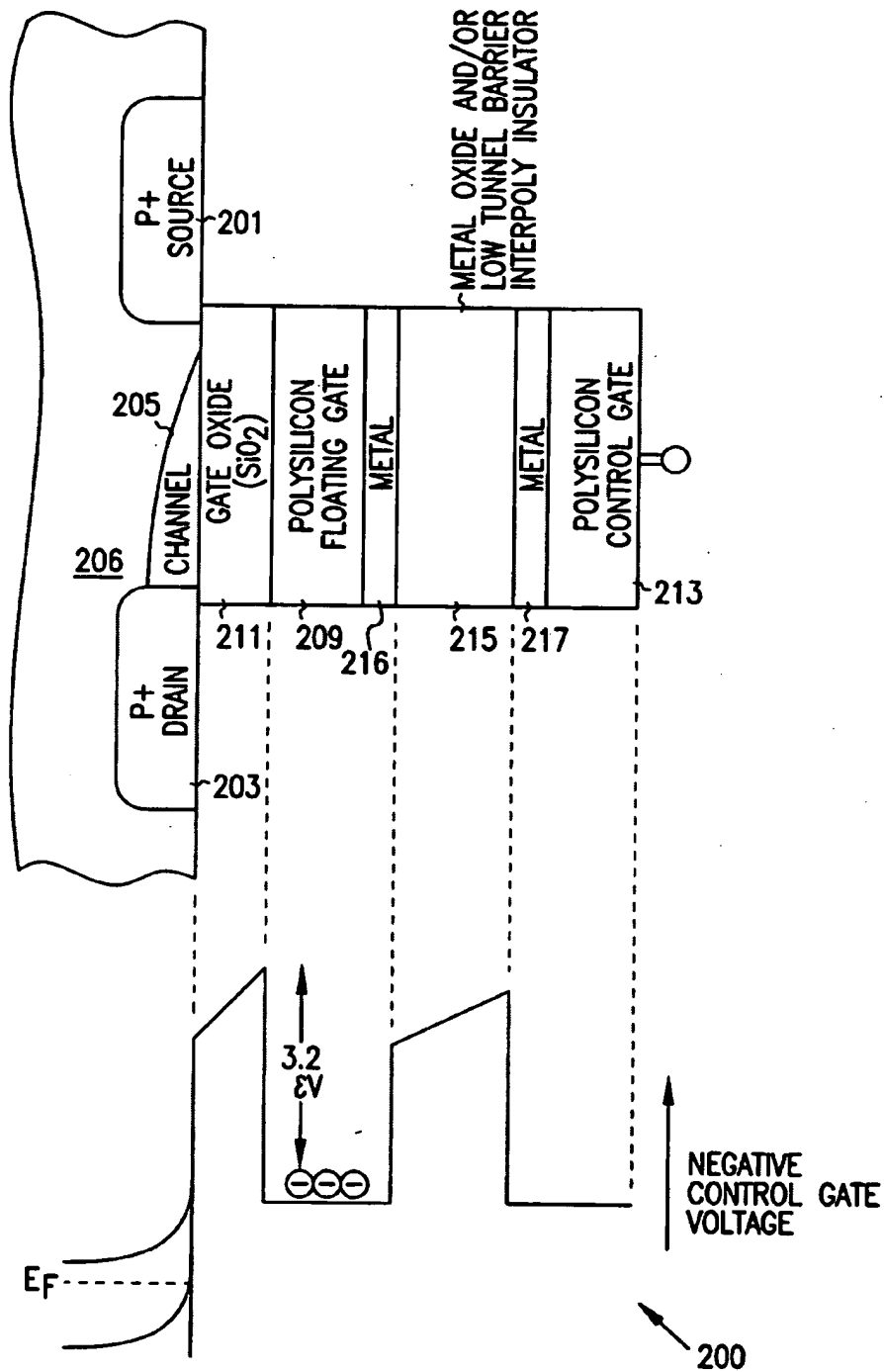


FIG. 2

TITLE: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND
ASYMMETRICAL TUNNEL BARRIERS

INVENTORS NAME: Leonard Forbes et al.

DOCKET NO.: 1303.035US1

3/17

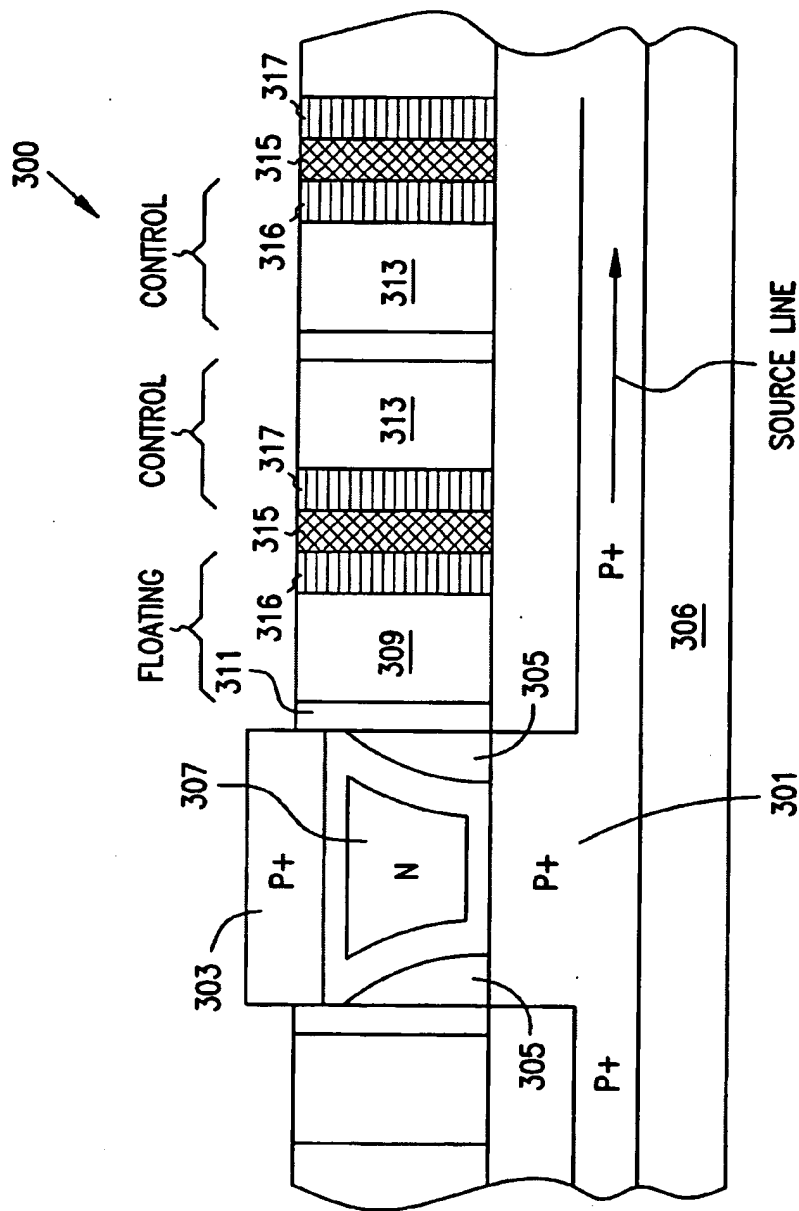


FIG. 3

INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.035US1

INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.035US1

DOCKET NO.: 1303.035US1

4/17

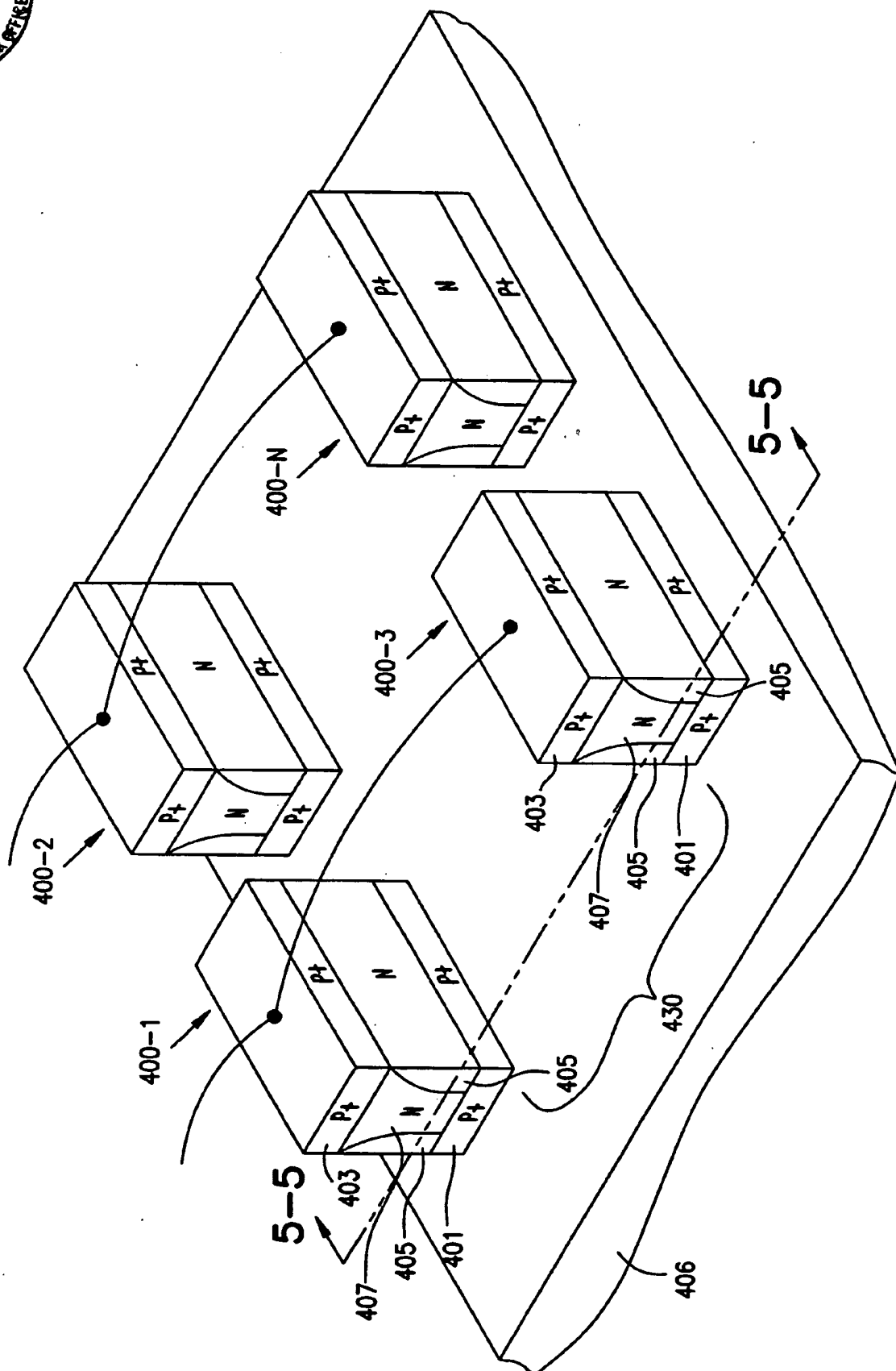


FIG. 4

TITLE: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND
ASYMMETRICAL TUNNEL BARRIERS

INVENTORS NAME: Leonard Forbes et al.

DOCKET NO.: 1303.035US1

5/17

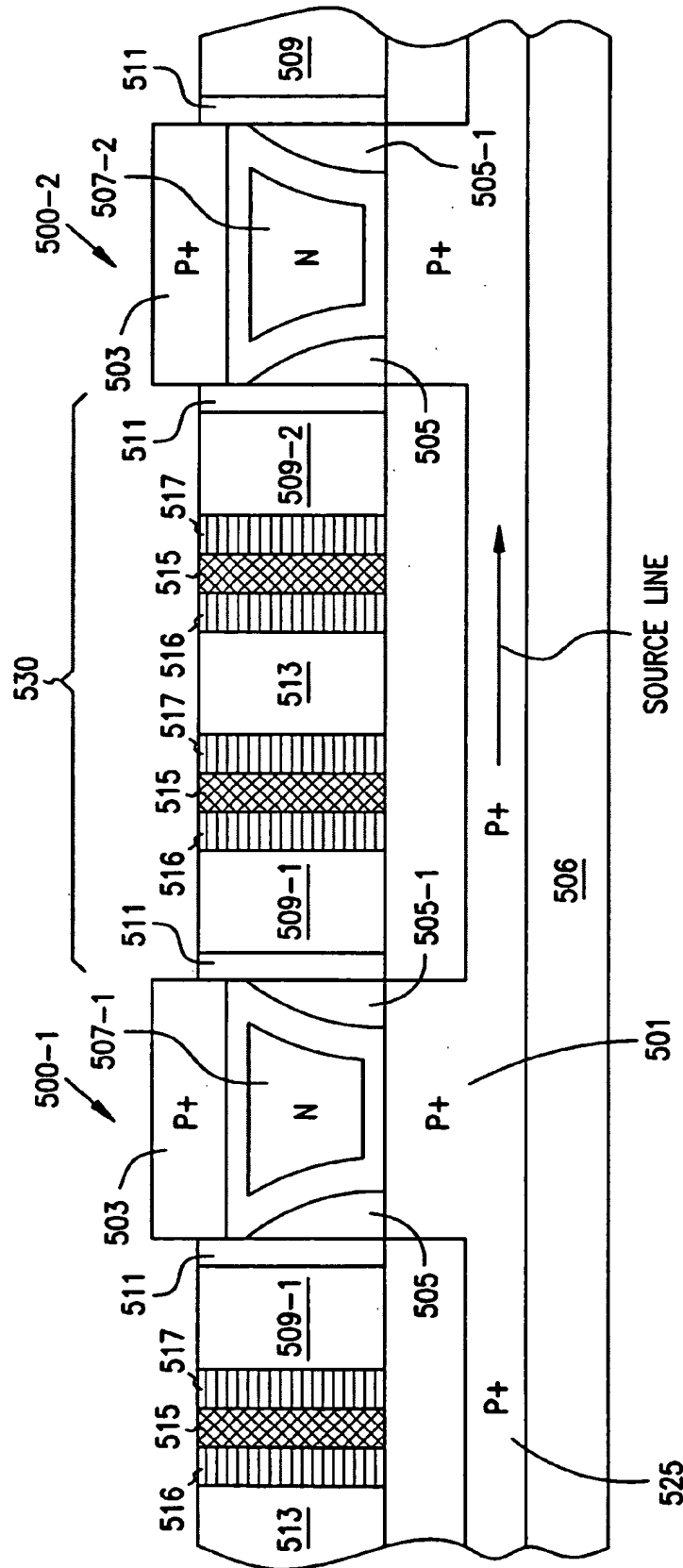


FIG. 5A

INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.035US1

6/17

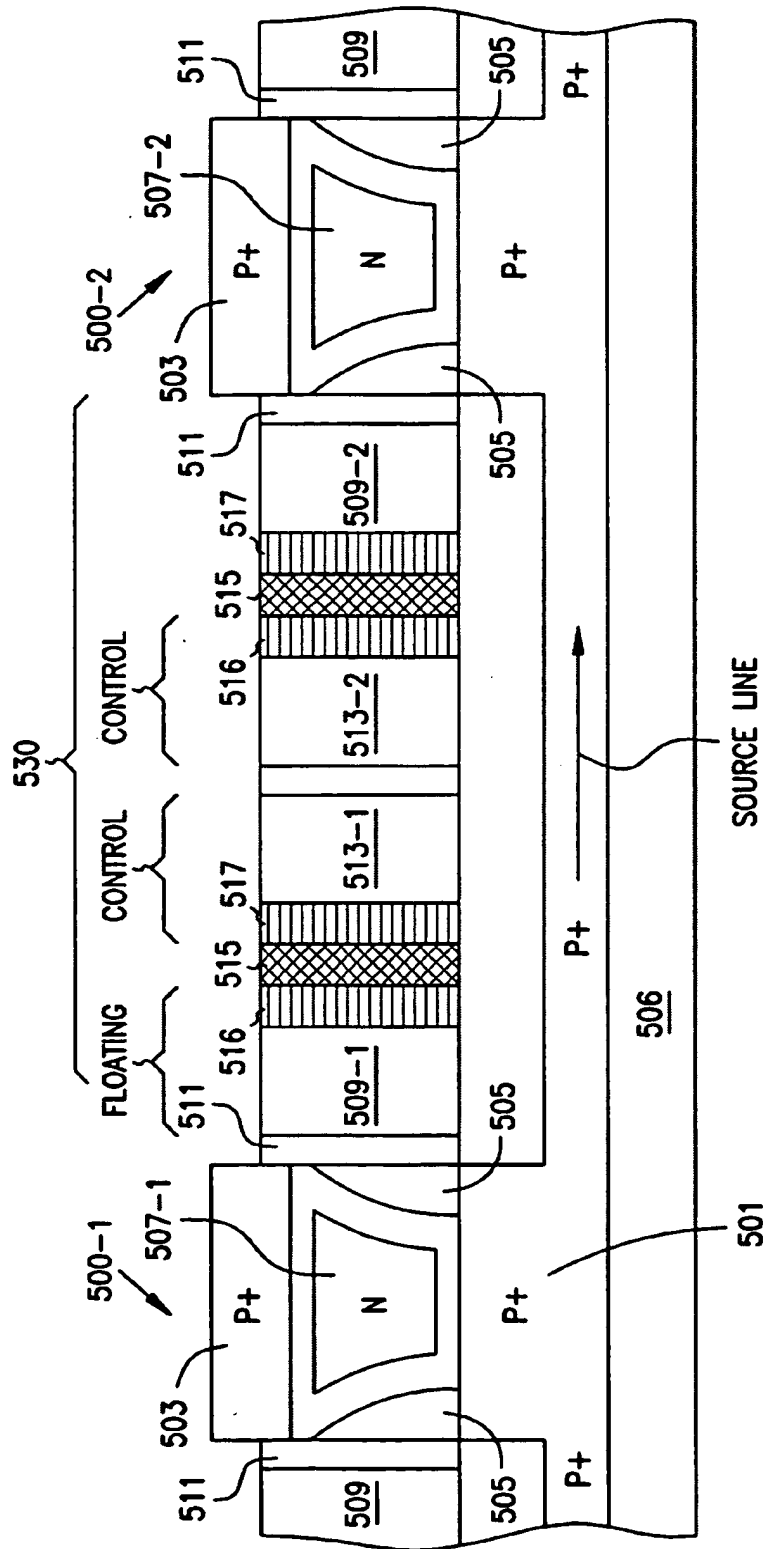


FIG. 5B

TITLE: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND
ASYMMETRICAL TUNNEL BARRIERS

INVENTORS NAME: Leonard Forbes et al.

DOCKET NO.: 1303.035US1

7/17

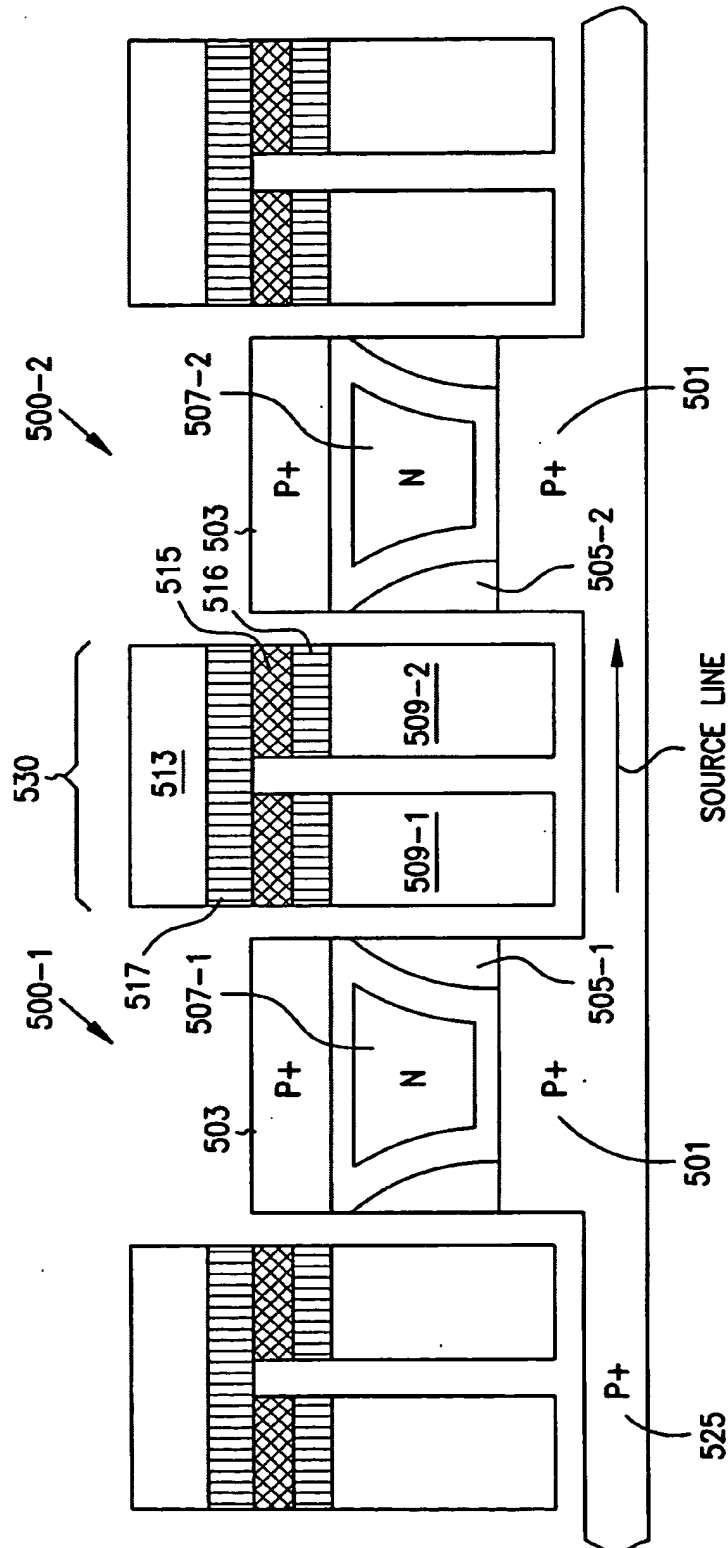


FIG. 5C

INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.035US1

DOCKET NO.: 1303.035US1

8/17

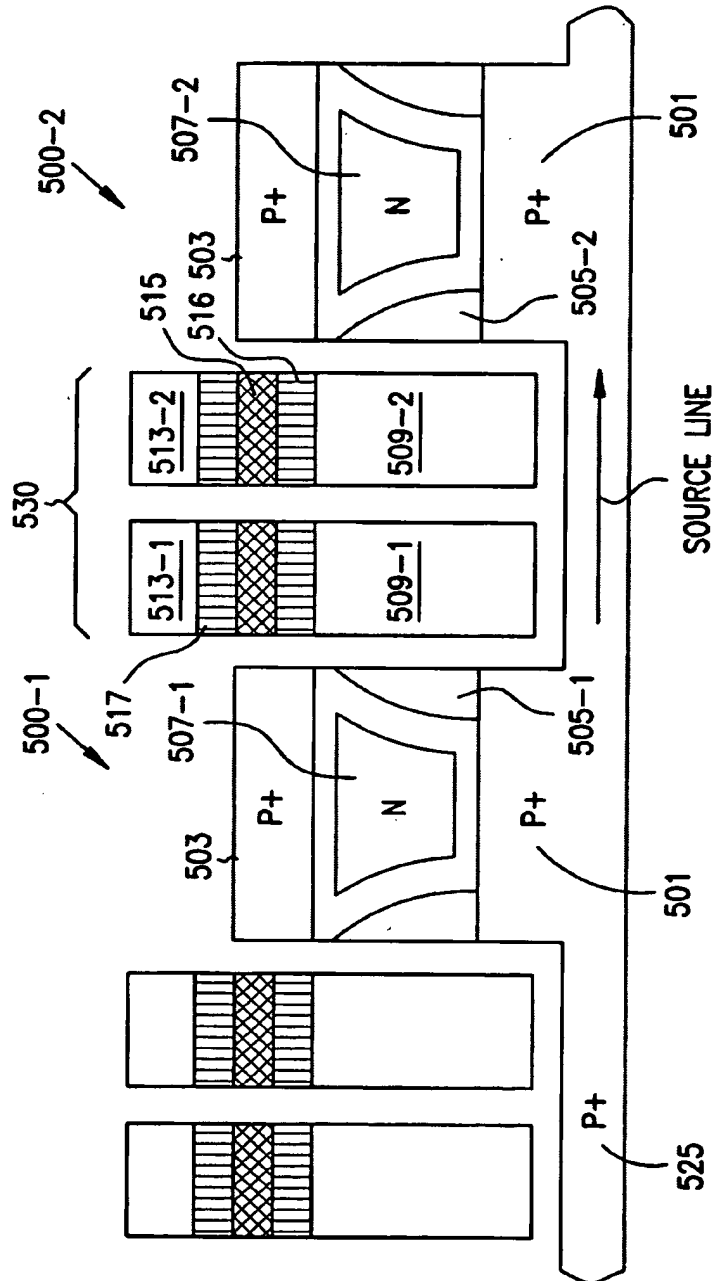
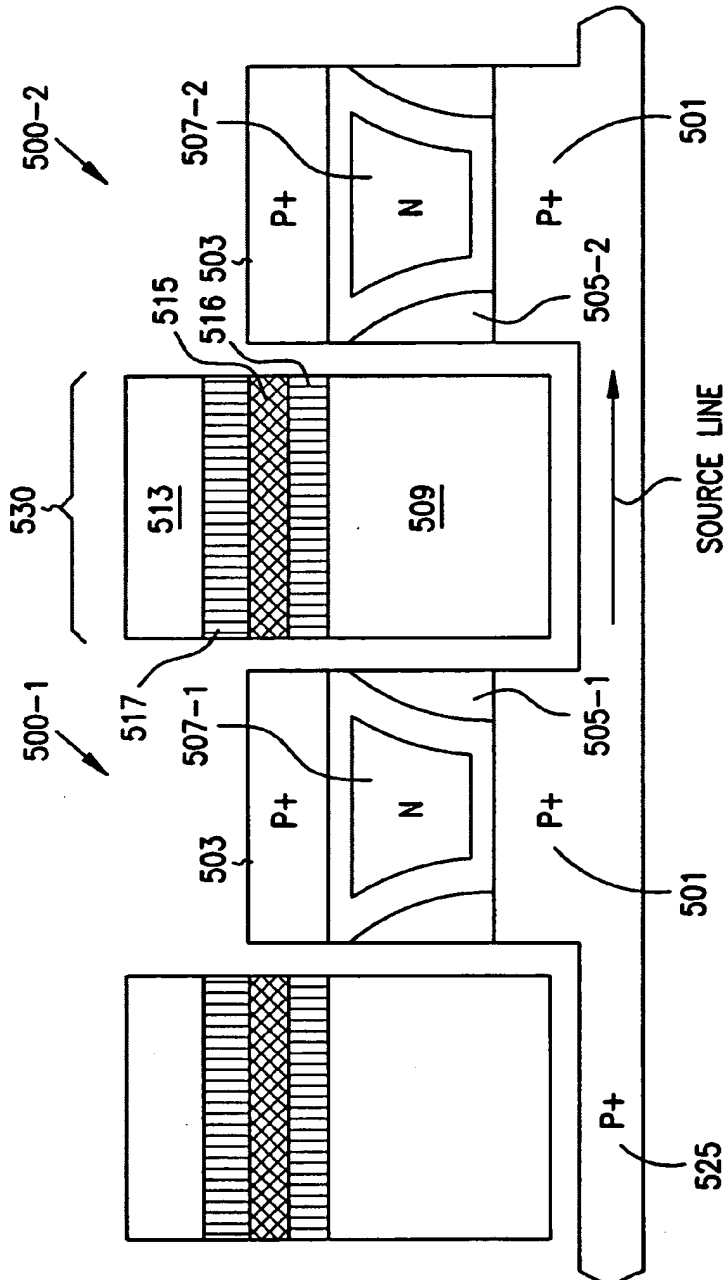


FIG. 5D

FIG. 5E



TITLE: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND
ASYMMETRICAL TUNNEL BARRIERS

INVENTORS NAME: Leonard Forbes et al.

DOCKET NO.: 1303.035US1

10/17

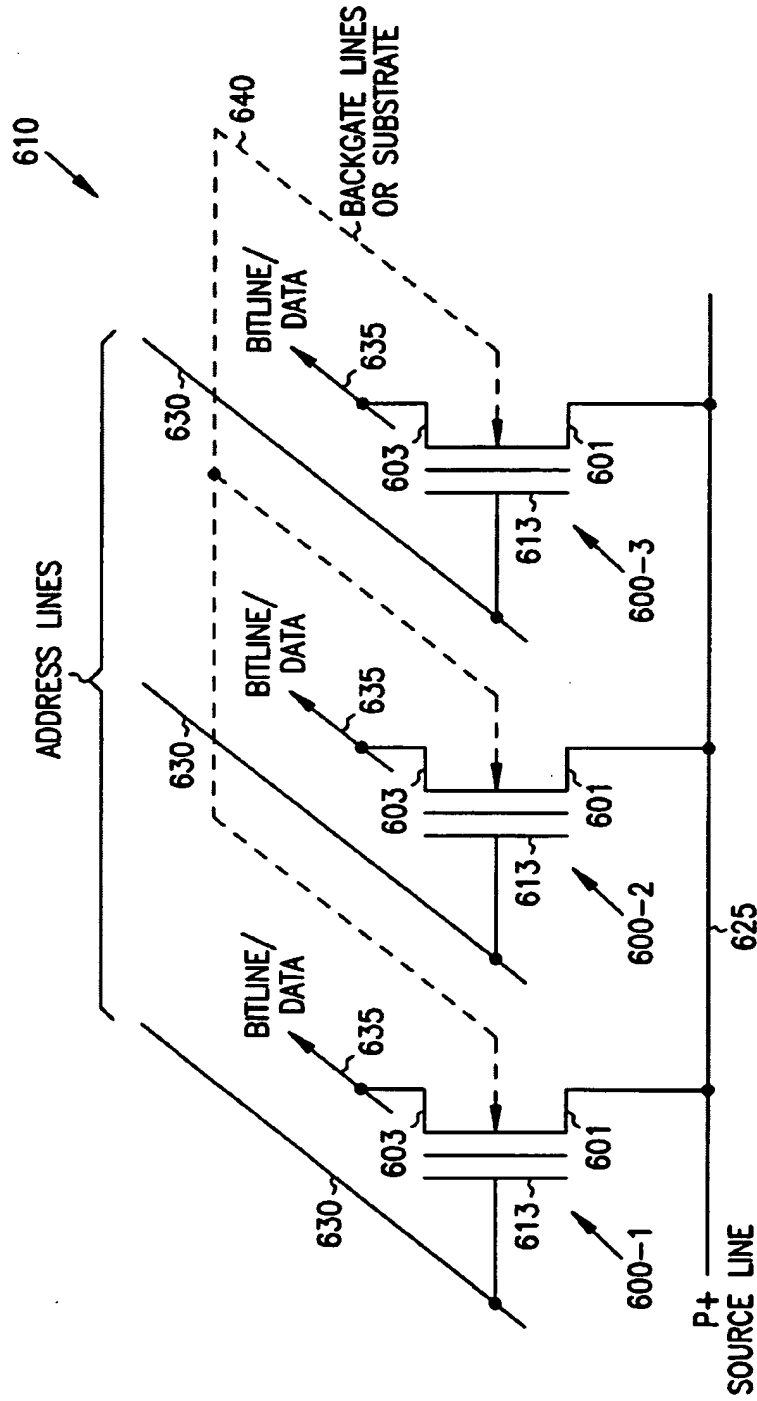


FIG. 6A

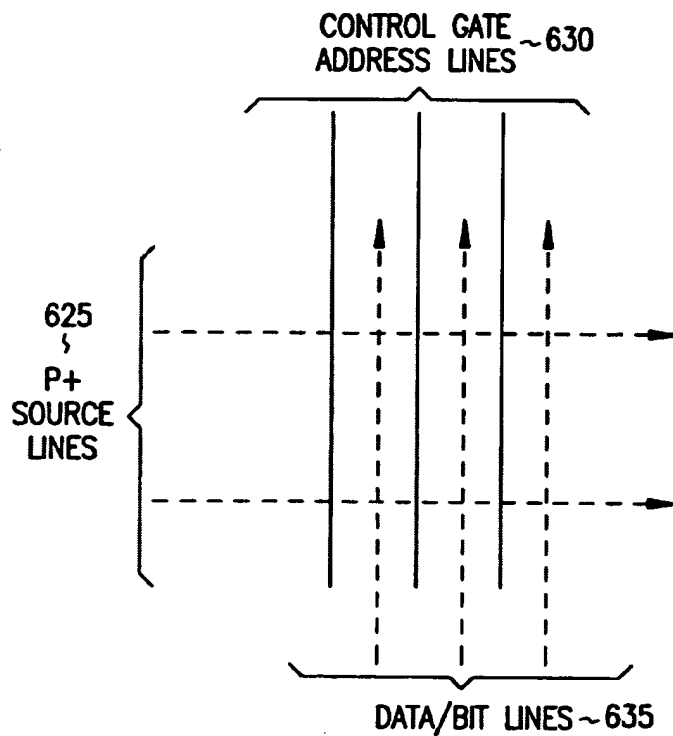


FIG. 6B

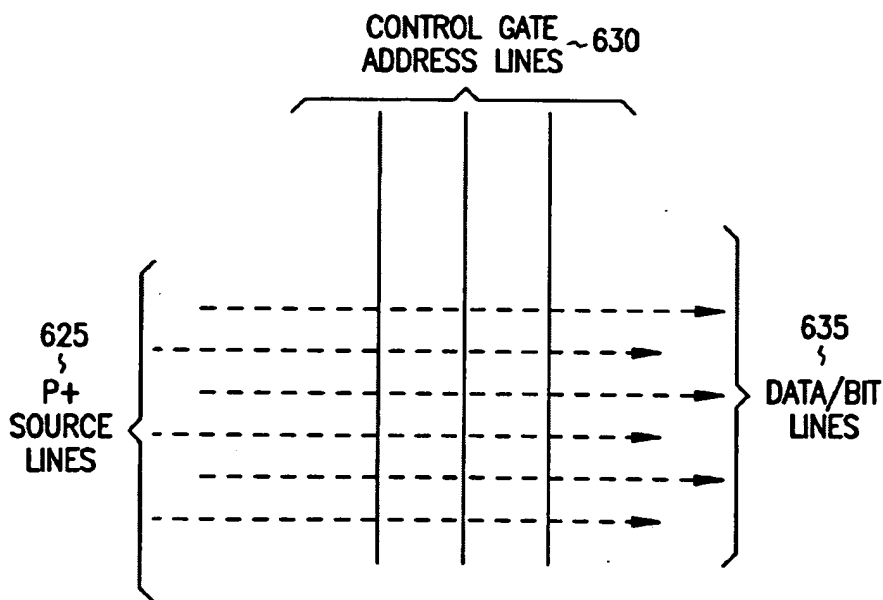


FIG. 6C

12/17

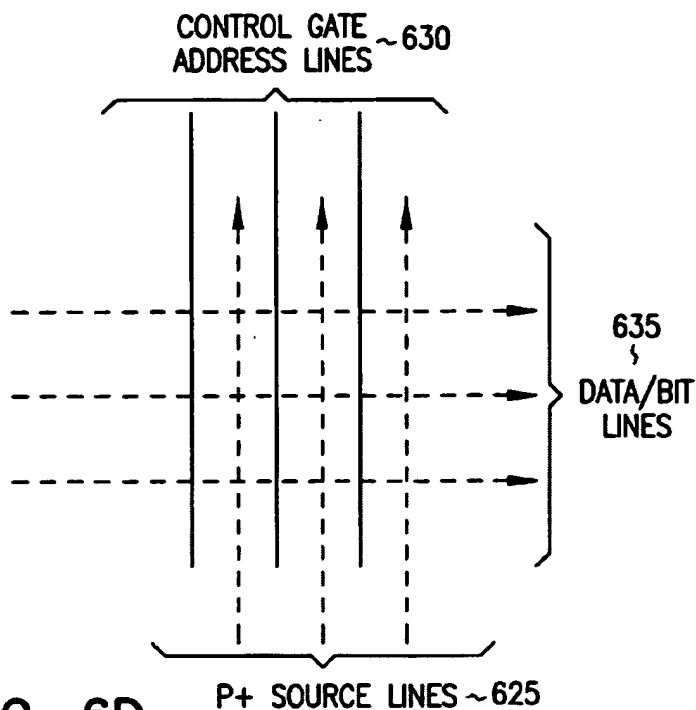


FIG. 6D

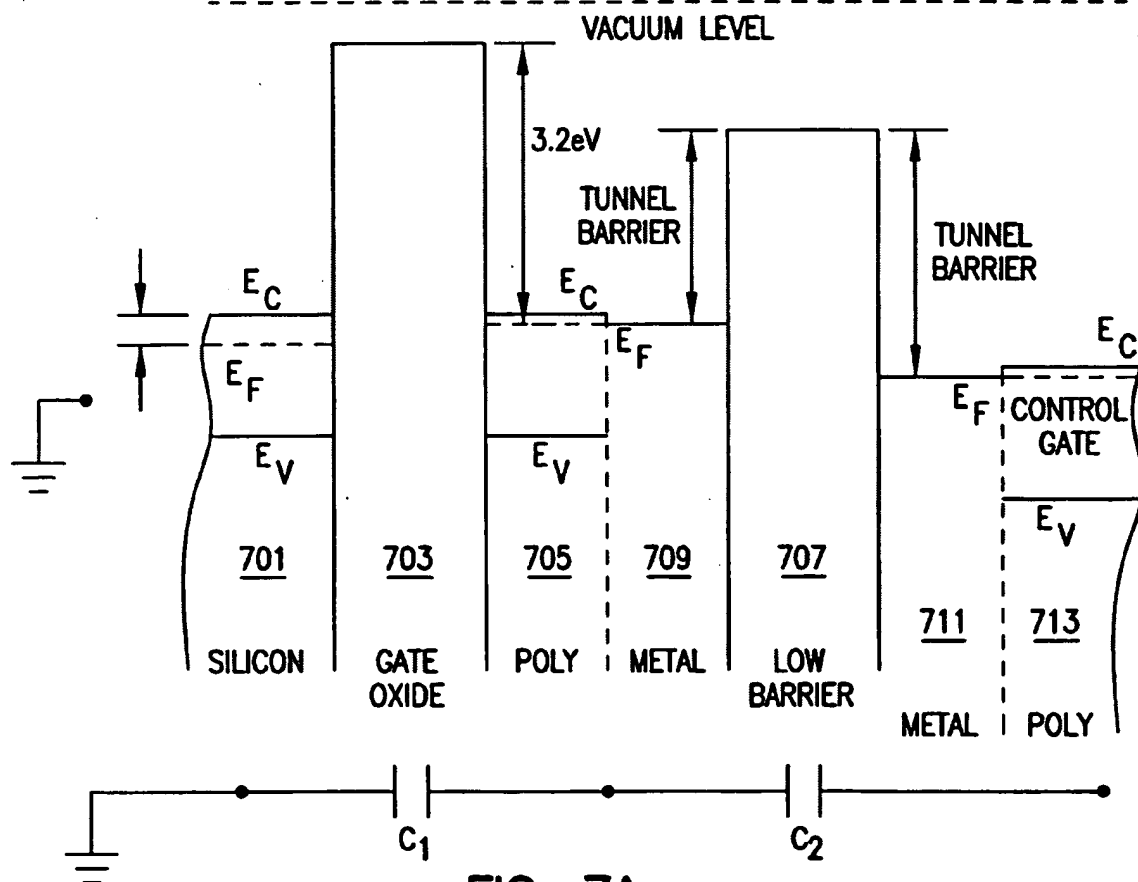


FIG. 7A

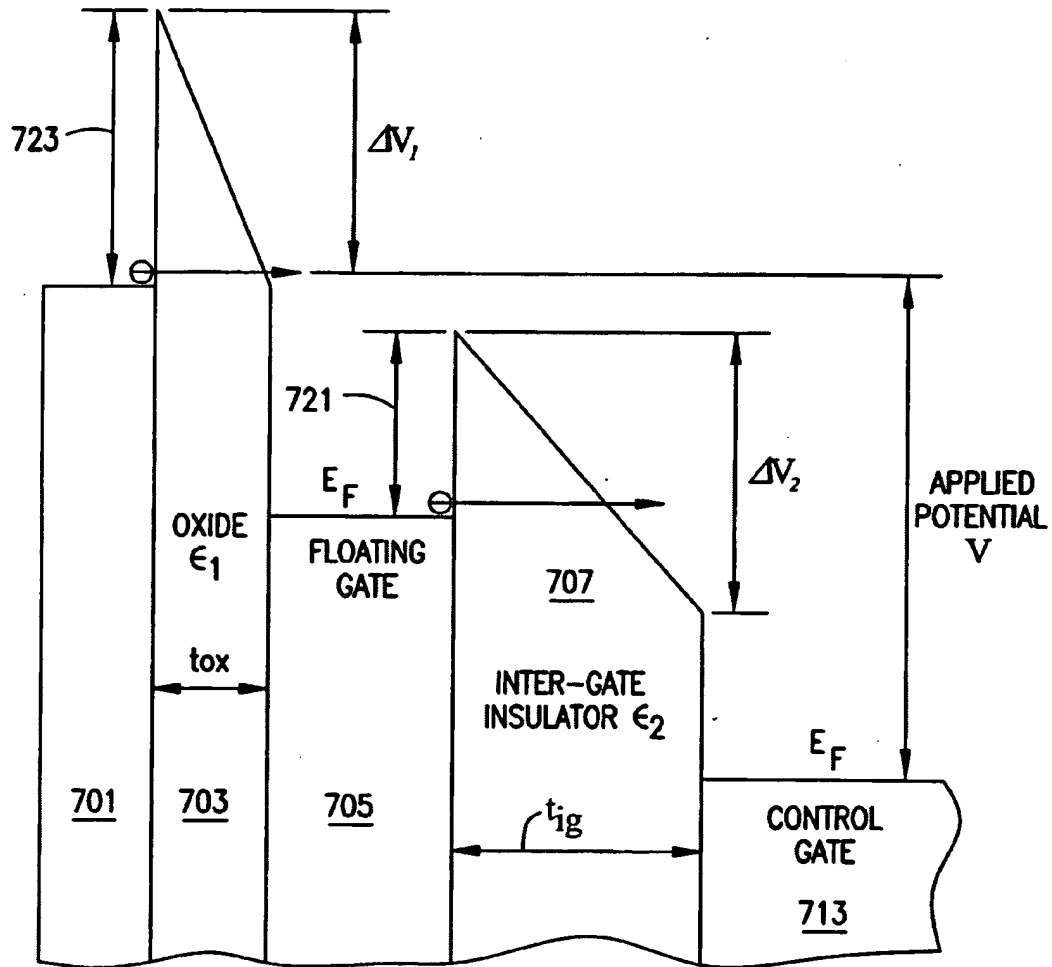


FIG. 7B



TITLE: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH F
ASYMMETRICAL TUNNEL BARRIERS
INVENTORS NAME: Leonard Forbes et
DOCKET NO.: 1303.035US1
14/17

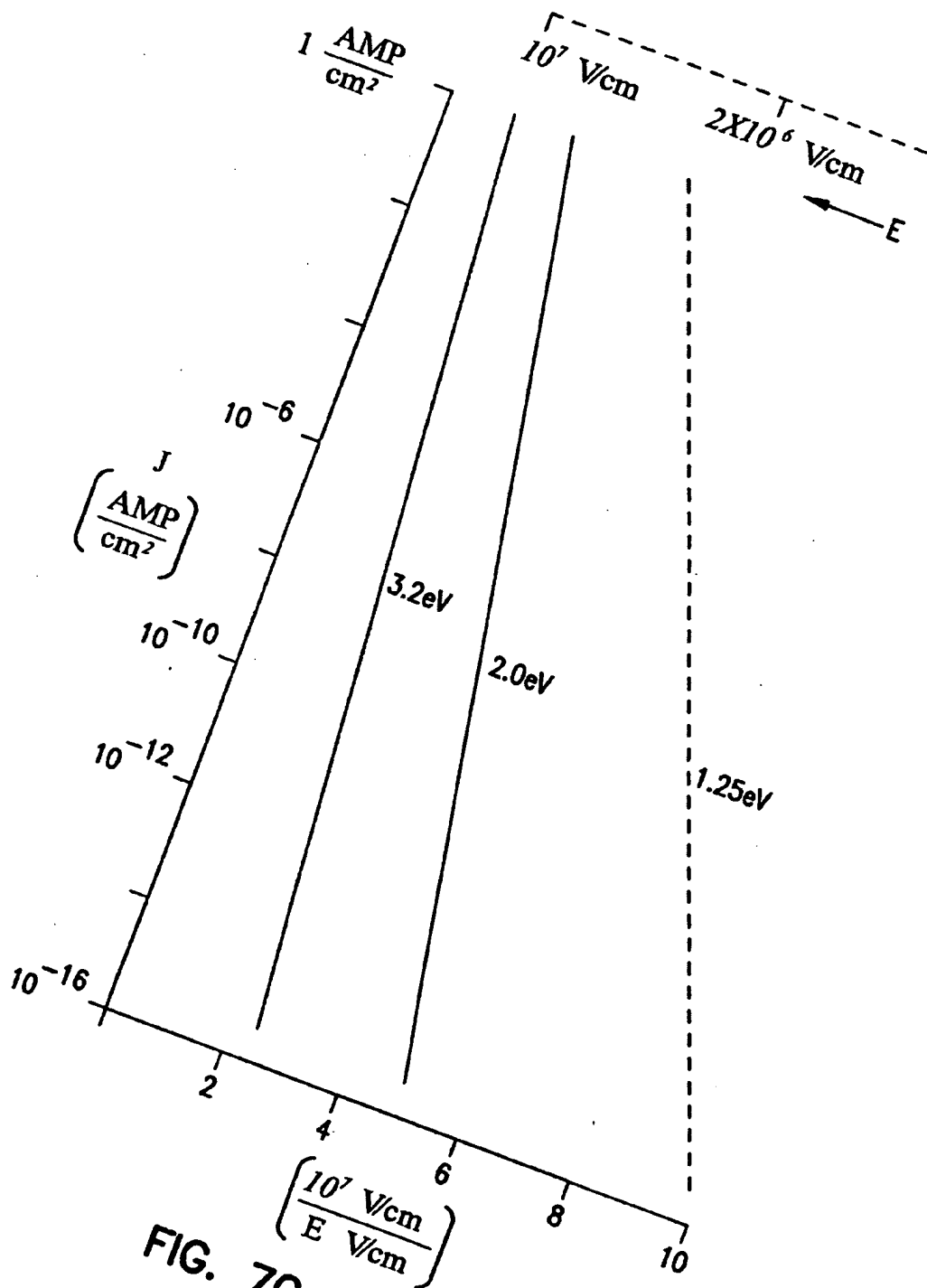


FIG. 7C

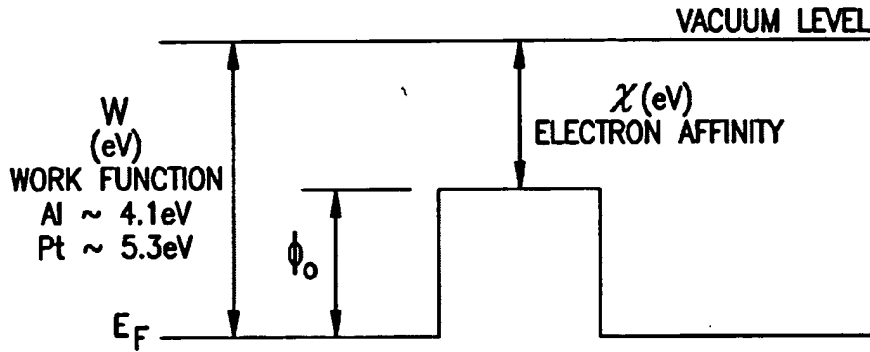


FIG. 8

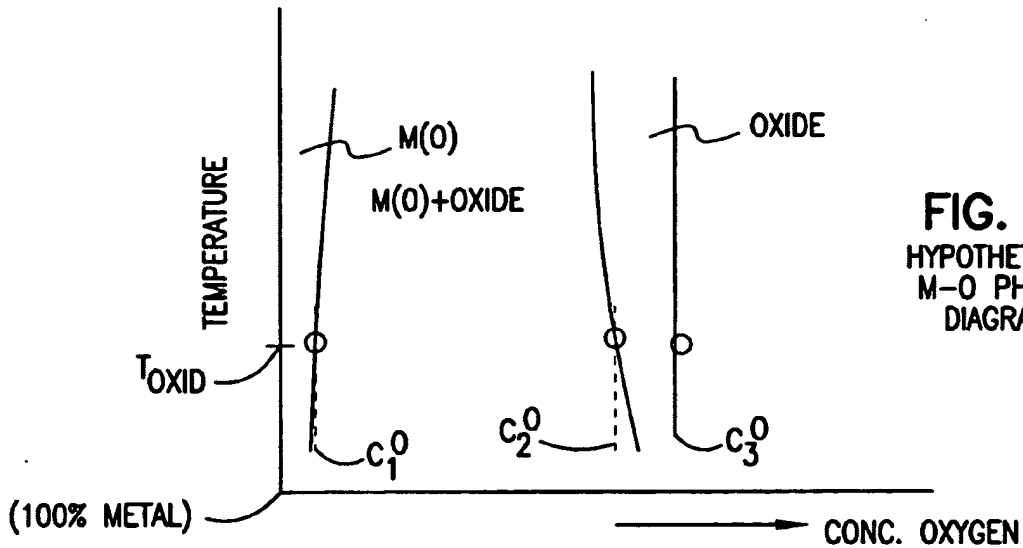
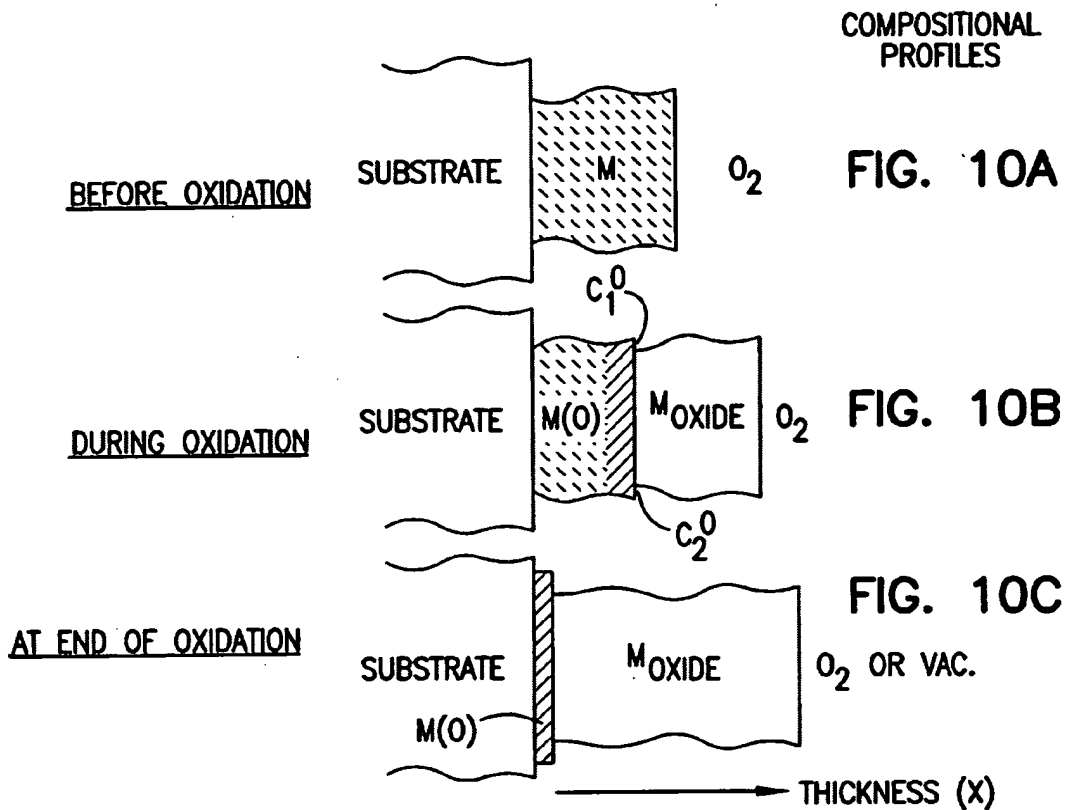


FIG. 9
HYPOTHETICAL
M-O PHASE
DIAGRAM



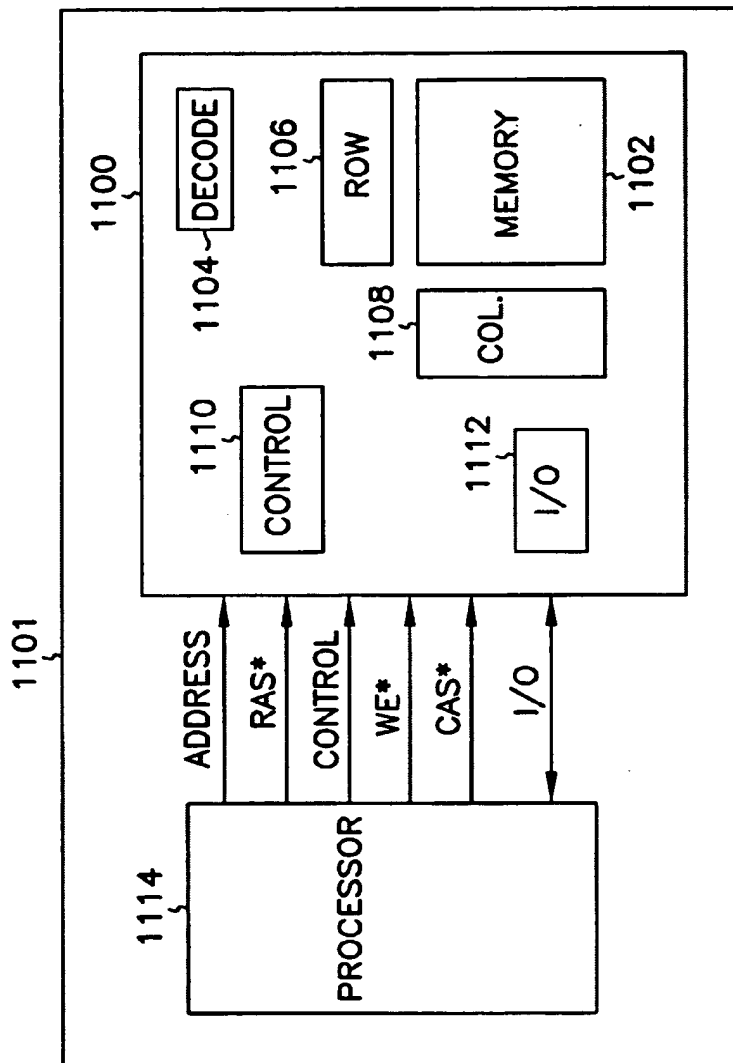


FIG. 11